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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HAMILL, ERIC R	

ART UNIT	PAPER NUMBER
2809	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/526,687	ENGEL ET AL.	
	Examiner	Art Unit	
	Eric R. Hamill	2809	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03-02-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6-10, 15, 16, and 20 are being rejected under 35 U.S.C. 102(b) as being anticipated by Devoe (US Patent Application Publication No. 5,657,199).

For claim 1, Devoe teaches: A resonance filter (See Abstract), comprising: at least three multilayer capacitors (Fig 2) having at least two different capacitances (Fig. 2), the at least three multilayer capacitors being adjacent each other (Fig. 2); wherein two capacitors of the at least three multilayer capacitors have a same capacitance (Column 12, lines 50-54), the two capacitors being on outer ends (Fig 2) of an arrangement formed by the at least three multilayer capacitors (Fig. 2).

For claim 2, Devoe further teaches the filter wherein the at least three multilayer capacitors (Fig 5) are connected in parallel (Fig.5).

For claim 3, Devoe further teaches the filter wherein the at least three multilayer capacitors (Fig. 2) comprise: a stack of dielectric layers (Fig. 2); and electrode layers

between dielectric layers in the stack (Fig. 2), the dielectric layers and the electrode layers forming a component (Fig. 2; See also Column 12, lines 50-54).

For claim 4, Devoe further teaches the filter of claim 3 wherein the external contacts on faces of the component (Fig. 1 shows external contacts on the face of the capacitor, the external contacts corresponding to electrode layers in the component), the external contacts corresponding to electrode layers in the component. (Column 12; Lines 43-46).

For claim 6, Devoe further teaches the filter of claim 3 wherein the component has a length and a width, the length being greater than the width (Fig. 3 and 4); and wherein electrode layers for different ones of the at least three multilayer capacitors are arranged substantially in parallel lengthwise in the component. (Fig. 3 and 4).

For claim 7, Devoe further teaches the filter of claim 3 wherein the component has a length and a width, the length being greater than the width (Fig. 3 and 4); and wherein electrode layers for different ones of the at least three multilayer capacitors are arranged substantially in parallel widthwise in the component. (Fig. 3 and 4)

For claim 8, Devoe further teaches the filter of claim 3 wherein the external electrodes on faces of the component. (Fig 6, elements 24a and 24b)

For claim 9, Devoe further teaches the filter of claim 3 wherein a connector element that is external to the component (Fig 2, elements 24a and 24b; column 13; Lines 54-55) and that connects the at least three multilayer capacitors. (Fig 2, elements 24a and 24b; column 13; Lines 54-55)

For claim 10, Devoe further teaches the filter of claim 1 wherein the at least three multilayer capacitors (Fig 2) comprise only three multilayer capacitors (Fig 2).

For claim 15, Devoe further teaches the filter of claim 3 wherein the cross-section of the component has a surface area that is less than 6 mm^2. (Column 4, line 3 describes the filter as being 0.070" x 0.070" x 0.020" thickness. This is equal to 1.778mm x 1.778mm or 3.16mm^2)

For claim 16, Devoe further teaches the filter of claim 1 wherein electrode layers (Fig. 3 and 4) for the two capacitors (Fig 3 and 4) have surface areas that are substantially same. (Fig. 3 and 4)

For claim 20, Devoe further teaches: A resonance filter comprising: a first charge storage device having multiple layers including an electrode layer (Fig. 2, element C1a); a second charge storage device having multiple layers including an electrode layer (Fig. 2, element C2); a third charge storage device having multiple layers including an electrode layer(Fig. 2; element C1a); a connecting element that connects the first,

second, and third charge storage devices in parallel (Fig 6 items 24a and 24b; column 13; Lines 54-55), the connecting element connecting to electrode layers of the first, second, and third charge storage devices (Fig 2 items 24a and 24b; column 13; Lines 54-55); wherein the second charge storage device is between the first charge storage device and the third charge storage device in an electrical sense (Fig. 2; C2) ; and wherein the first charge storage device and the third charge storage device have substantially identical electrical properties (Fig. 2; C1a, C2 and C1b) that are different from a corresponding electrical property of the second charge storage device (Fig 2 and Column 13, lines 1-3).

3. Claims 1, 11, 17-19 are being rejected under 35 U.S.C. 102(b) as being anticipated by **Yamada** (US Patent Application Publication No. 5,172,299).

For claim 1, Yamada teaches a filter (See Abstract. The term "resonance filter" is given its broadest reasonable interpretation which includes a multilayer capacitor) comprising: at least three multilayer capacitors (Fig 14) having at least two different capacitances (Fig. 14), the at least three multilayer capacitors being adjacent each other (Fig. 14); wherein two capacitors of the at least three multilayer capacitors have a same capacitance (Fig 14, see capacitors 94c and 94b. Note that the capacitance depends on the area of overlap between two electrodes. Therefore, capacitors 94b and 94c will have the same large capacitance), the two capacitors being on outer ends (Fig. 14, 94a and 94d) of an arrangement formed by the at least three multilayer capacitors (Fig. 14).

For claim 11, Yamada further teaches the filter of claim 1, wherein the at least three multilayer capacitors comprise four multilayer capacitors (Fig. 14), the four multilayer capacitors being in a parallel arrangement (Fig. 14), the four multilayer capacitors comprising two center capacitors (Fig 14, see capacitors 94c and 94b. Note that the capacitance depends on the area of overlap between two electrodes. Therefore, capacitors 94b and 94c will have the same large capacitance. Whereas, capacitors 94a and 94d will have the same small capacitance.) located between two edge capacitors (Fig 14, 94a and 94d) in the parallel arrangement (Fig. 2 and Fig. 3A and Fig 3B. Figure 2 shows elements 45 and 46 connecting the layers in parallel, and Figs. 3 and 4 show the capacitors, 42 and 44, being connected in parallel to a connector element labeled 42e and 44e.), the two center capacitors having a same capacitance (Fig. 14. Again, capacitors 94b and 94b have the same area of overlap. Therefore their capacitances will be the same).

For claim 17, Yamada teaches: A resonance filter (Abstract) comprising: plural capacitors (Fig 3A and 3B), each of the plural capacitors comprising alternating layers of dielectric and electrode (Fig. 2), the plural capacitors being arranged in parallel and interconnected (Figs. 2, 3A and 3B), the plural capacitors comprising:

a first outer capacitor having an electrode with a first surface area (Fig. 10, 54a);

a second outer capacitor having an electrode with the first surface area;(Fig. 10, 54d)

and one or more inner capacitors that are between the first outer capacitor (Fig. 10, 54b and 54c) and

the second outer capacitor in an electrical sense, the one or more inner capacitors having one or more corresponding electrodes with surface areas that are different than the first surface area.(Fig 10; See also Column 7, Lines 52-54)

For claim 18, Yamada further teaches the filter of claim 17, wherein the one or more inner capacitors (Fig 14; 94b and 94c) have a capacitance that is higher than a capacitance of the first outer capacitor (Fig 14, elements 94a and 94d have a smaller area of overlap than electrodes94b and 94c, therefore the capacitance of the outer electrodes will be higher).

For claim 19, Yamada further teaches the filter of claim 17, further comprising a connecting element (Fig 3A and 3B, 42e and 44e) that connects electrodes of the first outer capacitor, the second outer capacitor, and the one or more inner capacitors, the connecting element being electrically conductive (Fig 3A and 3B).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 5 is being rejected as being unpatentable over Devoe as applied to claim 3, above, further in view of Harada (Japanese Application Publication No. JP407201634A). Devoe teaches the limitation of claim 3 for the reasons above. Devoe differs from the claimed invention in that the filter is not taught to necessarily include an internal connector element to connect the at least three capacitors. Harada teaches a connector element to connect electrode layers of different ones of the at least three multilayer capacitors, the connector element being inside the component (Fig 2. elements 17 and 18; see also [0025 - 0026] describing holes 17 and 18 that are filled with a conductive paste used to internally connect the capacitive electrode layers). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have included a connector element to connect electrode layers of different ones of the at least three multilayer capacitors, the connector element being inside the component in the multilayer capacitor of Devoe, since Harada teaches that in order to prevent a "solder bridge"[0015] from forming when a ceramic chip is attached to a circuit board [0008], especially in surface mounting technology [0002], an internal

connector element is necessary ([0018]; See also [0021]) to prevent a "solder bridge" [0028].

6. Claim 13 is being rejected as being unpatentable over Devoe as applied to claim 3, above, further in view of Rayburn (US Patent Application Publication No. 3,617,834). Devoe teaches the limitation of claim 3 for the reasons above. Devoe differs from the claimed invention in that the filter is not taught to necessarily include dielectric layers comprising barium titanate-based ceramics. Rayburn teaches that multilayer capacitors are manufactured with dielectric layers comprising barium titanate-based ceramics (Column2, Lines 65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have used dielectric layers comprising barium titanate-based ceramics in the multilayer capacitor of Devoe, since Rayburn teaches that barium titanate based dielectric layers are used in order for a high potential to be sustained between the electrode layers of a multilayer capacitor. (Column 2; line 60-63).

7. Claim 14 is being rejected as being unpatentable over Devoe as applied to claim 3, above, further in view of Gupta (US Patent Application Publication No. 4,729,058). Devoe teaches the limitation of claim 3 for the reasons above. Devoe differs from the claimed invention in that the filter is not taught to necessarily include "electrode layers comprise a ceramic material having a varistor effect." Gupta teaches that filters are manufactured with electrode layers comprise a ceramic material having a varistor effect

(Column 1, Lines 10-20) Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have used electrode layers comprising a ceramic material having a varistor effect in the filter of Devoe in order to protect against high voltage surges by using thin films of ZnO-based ceramic dielectric material. (Column 1, Lines 10-20; See also Column 4, Lines 44-51).

8. Claim 12 is being rejected as being unpatentable over Devoe as applied to claim 1, above, further in view of Kaneko (US Patent Application Publication No. 4,947,286). Devoe teaches the limitation of claim 1 for the reasons above. Devoe differs from the claimed invention in that the filter is not taught to necessarily include leads that interconnect the at least three multilayer capacitors; and inductors connected to the leads. Kaneko teaches that noise filters are manufactured with leads (Fig. 4, elements 26c to 29c; see also Column 5, Lines 20-25) that interconnect the at least three multilayer capacitors (Fig. 4 elements 26a to 29a and 26b to 29b; and Column 4, Lines 10-13); and inductors connected to the leads (Fig 4, elements 26d to 29e and elements 26e –29e; See also Fig. 7 which shows that these inductors are connected to the leads). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have leads that interconnect the at least three multilayer capacitors; and inductors connected to the leads in the filter of Devoe, since Kaneko teaches that in order to have a noise filter with reduced insertion loss in the high frequency band (Column 5, Lines 21-24) inductors are used to connect the at least three multilayer capacitors to the leads [0006].

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tokuda (Japanese Application Publication No. JP407161576A) teaches leads that interconnect the at least three multilayer capacitors; and an inductor connected to the leads.

10. Any response to this Office Action should be **faxed** to (571) 273-8300 or **mailed** to:

Commissioner for Patents,
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-Delivered responses should be brought to
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Hamill, whose telephone number is (571) 270-1802. The examiner can normally be reached Mon-Fri from 7:30-5:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benny Q. Tieu, can be reached at (571) 272-7490. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have question on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric Hamill

Patent Examiner Art Unit 2809

BENNY Q. TIEU
SPE/ TRAINER